REMARKS

This is a full and timely response to the outstanding final Office Action mailed August 28, 2006. Reconsideration and allowance of the application and pending claims are respectfully requested.

I. Claim Rejections - 35 U.S.C. § 112, Second Paragraph

Claims 1-21 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In particular, it is stated that claims 1, 6, 11, and 15 do not comprise limitations that support the claimed "evaluating a processor design". Applicant respectfully disagrees.

In each claim, recited are various actions, components, logic or means that all relate to and comprise a part of evaluating a processor design. For example, regarding claim 1, the processor design evaluation involves each of testing a lot of wafers at two or more voltage levels, collecting test results from the testing of the lot of wafers in a test results file, searching the test results file that contains the test results for the lot of wafers at the two or more voltage levels, and determining an optimal operational voltage based on test failures indicated in the test results. Each of those actions is performed in evaluating the processor design.

Applicant further notes that each of claims 1, 6, 11, and 15 use the "open" format through use of the term "comprising". With such a format, the limitations that follow must simply comprise part of the evaluation. There is no requirement that Applicant identify each specific aspect involved in the evaluation.

In view of the above, it is respectfully asserted that the claims define the invention in the manner required by 35 U.S.C. § 112. Accordingly, Applicant respectfully requests that the rejections to these claims be withdrawn.

II. Claim Rejections - 35 U.S.C. § 102(e)

Claims 1-4, 6-8, 11, and 14-21 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Ando* (U.S. Pub. No. 2004/0111231). Applicant respectfully traverses this rejection.

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(e).

In the present case, not every feature of the claimed invention is represented in the Ando reference. Applicant discusses the Ando reference and Applicant's claims in the following.

A. The Ando Disclosure

Ando discloses a method for obtaining system performance data by testing a discrete system at different supply voltages. As described by Ando, tests can be performed on "a wafer" or on individual chips of that wafer to evaluate the chips. *Ando*, paragraph 0026. As also described by Ando, "[t]he test typically consists of determining whether the chip can successfully execute one or more programs at various clock speeds, supply voltages, body-bias voltages, and programs of instruction sets at various temperatures." *Id.*

B. Applicant's Claims

As noted above, Ando fails to teach several of Applicant's claim limitations. Applicant discusses some of those claim limitations in the following.

1. Claims 1-5 and 16

Applicant's claim 1 provides as follows (emphasis added):

> 1. A method for evaluating a processor design, the method comprising:
>
> testing *a lot of wafers* at two or more voltage levels;
>
> *collecting test results from the testing of the lot of wafers in a test results file*;
>
> searching the test results file that contains the test results for the lot of wafers at the two or more voltage levels; and
>
> *determining an optimal operational voltage* based on test failures indicated in the test results.

Regarding claim 1, Ando does not teach testing "a lot of wafers" at different voltage levels. Instead, Ando only discusses testing "a wafer" or individual chips obtained from that wafer. Accordingly, Ando's evaluation is based on less information than that described in relation to claim 1. Regardless, Ando's lack of teaching as to testing "a lot of wafers" means that the Ando reference does not anticipate *each and every* limitation of claim 1.

As a further matter, Ando does not teach "collecting test results from the testing of the lot of wafers in a test results file". Again, since Ando does not test an entire "lot" of wafers, Ando does not collect test results from a "lot" of wafers in a single file. Hence, Ando's test results file contains much less information.

Furthermore, Ando does not actually teach "determining an optimal operational voltage based on test failures indicated in the test results". Although, as noted above, Ando performs testing at various supply voltages, *nowhere* does Ando state that an "optimal operational voltage" is determined. The Ando reference cannot anticipate claim 1 for that reason also. Applicant further notes that just because Ando tests at various supply voltages, this does not necessarily mean that Ando makes a determination as to which is optimal. For example, the various different supply voltages could simply be used as different input conditions to evaluate the other characteristics, such as clock speeds and programs of instruction sets at various temperatures, as described in paragraph 0026 of the Ando reference.

Regarding dependent claim 4, Ando does not actually teach "determining the number of test failures" at a first and second voltage level or "determining which of the first voltage level and the second voltage level had the least test failures". Although Ando speaks of conducting testing at various supply voltages, nowhere does Ando describe determining "the number of test failures" at those particular voltages.

Regarding dependent claim 16, Ando further does not actually teach "determining the relative significance of the test failures and determining the optimal operational voltage based upon the relative significance". Again, Ando does not describe determining any "optimal operation voltage". Further, Ando does not describe determining the "relative significance of the test failures". Applicant has reviewed paragraph 0027 of the Ando reference identified in the Office Action and can find no such teaching. Applicant requests that the Examiner identify with specificity which sentences of that paragraph actually teach determining the "relative significance of the test failures".

2. Claims 6-10, 17, and 18

Applicant's claim 6 provides as follows (emphasis added):

> 6. A system for evaluating a processor design, the system comprising:
>
> *a component configured to test a lot of wafers at two or more voltage levels and collect test results from the testing of the lot of wafers in a test results file*;
>
> a parser module configured to search the test results file that contains the test results for the lot of wafers at the two or more voltage levels;
>
> *a test failure calculation module configured to determine test failures that occurred at the two or more voltage levels*; and
>
> *an optimal operational voltage module configured to determine which of the two or more voltage levels is optimal.*

Regarding claim 6, Ando teaches none of: a component configured to test "a lot of wafers" and "collect test results from the testing of the lot of wafers in a test results file", a test failure calculation module "configured to determine test failures that occurred at the two or more voltage levels", or an optimal operational voltage module "configured to determine which of the two or more voltage levels is optimal" for reasons described above.

Regarding dependent claim 17, Ando does not teach a module "configured to determine the number of test failures at a first voltage level, determine the number of test failures at a second voltage level, and determine which of the first voltage level and the second voltage level had the least test failures" for reasons described above.

Regarding dependent claim 18, Ando does not teach a module "configured to determine the relative significance of the test failures and determine the optimal operational voltage based upon the relative significance" for reasons described above.

3. Claims 11-14 and 19

Applicant's claim 11 provides as follows (emphasis added):

> 11. A computer program embodied in a computer-readable medium for evaluating a processor design, the program comprising:
>
> *logic configured to test a lot of wafers at two or more voltage levels and collect test results from the testing of the lot of wafers in a test results file*;
>
> logic configured to search the test results file that contains the test results for the lot of wafers at the two or more voltage levels; and
>
> *logic configured to determine an optimal operational voltage based on test failures indicated in the test results.*

Regarding claim 11, Ando does not teach either of logic configured to test "a lot of wafers" and collect test results from the testing of the lot of wafers in a test results file, or logic configured to "determine an optimal operational voltage based on test failures indicated in the test results" for reasons described above.

Regarding dependent claim 14, Ando does not teach logic configured to "determine the number of test failures at a first voltage level; determine the number of test failures at a second voltage level; and determine which of the first voltage level and the second voltage level had the least test failures" for reasons described above.

4. Claims 15, 20, and 21

Applicant's claim 15 provides as follows (emphasis added):

> 15. A system for evaluating a processor design, the system comprising:
>
> *means for testing a lot of wafers at two or more voltage levels*;
>
> *means for collecting test results from the testing of the lot of wafers in a test results file*;
>
> means for searching the test results file that contains the test results for the lot of wafers at the two or more voltage levels; and
>
> *means for determining an optimal operational voltage based on test failures indicated in the test results.*

Regarding claim 15, Ando does not teach any of means for testing "a lot of wafers" at two or more voltage levels, means for "collecting test results from the testing of the lot of wafers in a test results file", or means for "determining an optimal operational voltage based on test failures indicated in the test results" for reasons described above.

Regarding dependent claim 20, Ando does not teach means for "determining the number of test failures at a first voltage level", "determining the number of test failures at a second voltage level", or "determining which of the first voltage level and the second voltage level had the least test failures" for reasons described above.

Regarding dependent claim 21, Ando does not teach means for "determining the relative significance of the test failures and determine the optimal operational voltage based upon the relative significance" for reasons described above.

III. Claim Rejections - 35 U.S.C. § 103(a)

As has been acknowledged by the Court of Appeals for the Federal Circuit, the U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a *prima facie* case of obviousness by showing some objective teaching in the prior art or generally available knowledge of one of ordinary skill in the art that would lead that individual to the claimed invention. *See In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). The Manual of Patent Examining Procedure (MPEP) section 2143 discusses the requirements of a *prima facie* case for obviousness. That section provides as follows:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.

In the present case, the prior art at least does not teach or suggest all of the claim limitations.

A. Rejection of Claims 5, 9, 12, and 13

Claims 5, 9, 12, and 13 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ando* in view of *Huang, et al.* ("Huang," U.S. Pub. No. 2003/0056029) and/or *Pugh* (U.S. Pub. No. 2002/0143785). Applicant respectfully traverses this rejection.

As identified above, Ando does not teach aspects of Applicant's claims. In that Huang and Pugh do not remedy the deficiencies of the Ando reference, Applicant respectfully submits that claims 5, 9, 12, and 13 are allowable over the Ando/Huang/Pugh combination for at least the same reasons that claims 1, 6, and 11 are allowable over Ando.

B. Rejection of Claim 10

Claim 10 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ando* in view of *Katla, et al.* ("Katla," U.S. Pub. No. 2005/0050480) and/or *Wookey, et al.* (U.S. Pat. No. 6,182,249). Applicant respectfully traverses this rejection.

As is identified above, Ando does not teach aspects of Applicant's claims. In that Katla and Wookey do not remedy the deficiencies of the Ando reference, Applicant respectfully submits that claim 10 is allowable over the Ando/Katla/Wookey combination for at least the same reasons that claim 6 is allowable over Ando.

IV. Canceled Claims

Claim 19 has been canceled from the application without prejudice, waiver, or disclaimer. Applicant reserves the right to present that canceled claim, or variants thereof, in continuing applications to be filed subsequently.

CONCLUSION

Applicant respectfully submits that Applicant's pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, Virginia 22313-1450, on

10-16-06

Mary Meegan

Signature